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REPORT

CEEFAX: microprocessor–based clock

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Summary

When CEEFAX became a public service it was necessary to provide a dependable source of clock-time for transmission as part of the signal. This report describes the principles used in the design of the master clock coupled to the CEEFAX computer.

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Research Department, Engineering Division,
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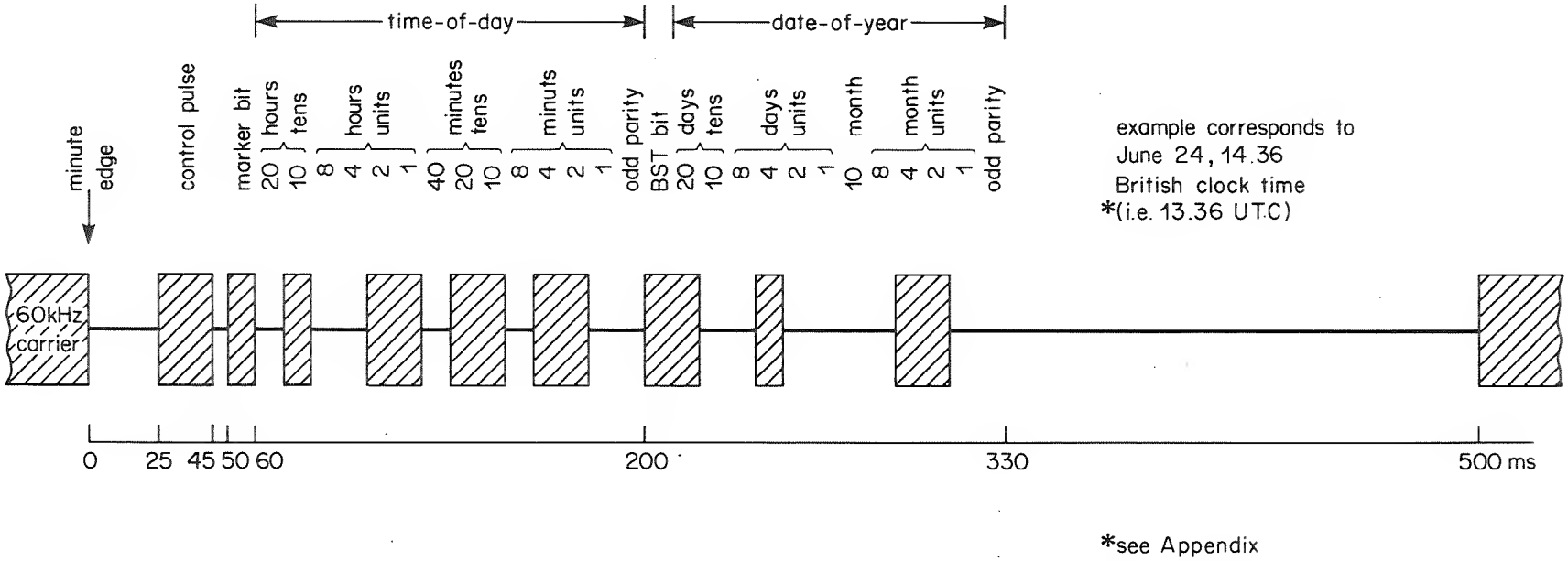

Fig. 1 - The 'fast' MSF time code

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1. Introduction

CEEFAX, the BBC system for broadcasting information in coded form during the television field-blanking interval, is now a full public service. A feature of the system is the display of the current clock-time, including seconds, in the corner of each page. In some circumstances the selection of pages for transmission is also based on clock time.

In order to offer a totally dependable source of time for these purposes it was decided that a clock would be designed and built specially for this application, combining the accuracy of the stable frequency sources available within a television studio centre with the absolute time setting available from the 60 kHz transmitter (MSF) at Rugby.

The design of this clock was used as an opportunity to assess the advantages of using a microprocessor in place of the many discrete logic gates and counters that would otherwise have been needed.

2. Requirement

The clock rate is determined by a 5 MHz signal, related to a Rubidium frequency standard, available at the BBC Television Centre, this signal is reliable and of more than adequate accuracy (of the order of 1 ms per year). The input to the clock is monitored to provide a rapid detection of its failure, and to discriminate against other signals which might inadvertently be applied instead (such as 4·43 MHz colour subcarrier). In the absence of the 5 MHz input the clock operates from an internal 5 MHz crystal oscillator which can be manually adjusted against the received 60 kHz standard frequency, to give a drift of less than 100 ms per day. The switching to and from the external 5 MHz reference, which is automatically selected when available, is arranged to cause negligible disturbances to the operation of the clock.

The clock setting is determined by the 'fast' time and date code (Fig. 1) controlled by the National Physical Laboratory, which is radiated every minute by the Post Office 60 kHz transmitter (MSF) at Rugby. The carrier is switched off (logic '0') and on (logic '1') at a signalling rate of 100 bit/s to give the month, day-of-month, hour and minute of the minute that has just begun. The UTC time scale (see Appendix) is used. An additional single bit indicates whether the current British clock-time is GMT or BST.

A very dependable means of interpreting this code is required, to be proof against interference; this is discussed in more detail below. To allow manual setting of the clock under unusual conditions, a keyboard is provided but it is only operative from power-on or key-controlled reset until an MSF time code has been correctly decoded. A photograph of the equipment is shown in Fig. 2. In normal operation, the clock is reset every minute when a time code is correctly decoded, although no action is taken if the error is less than about 3 ms. When the transmissions are

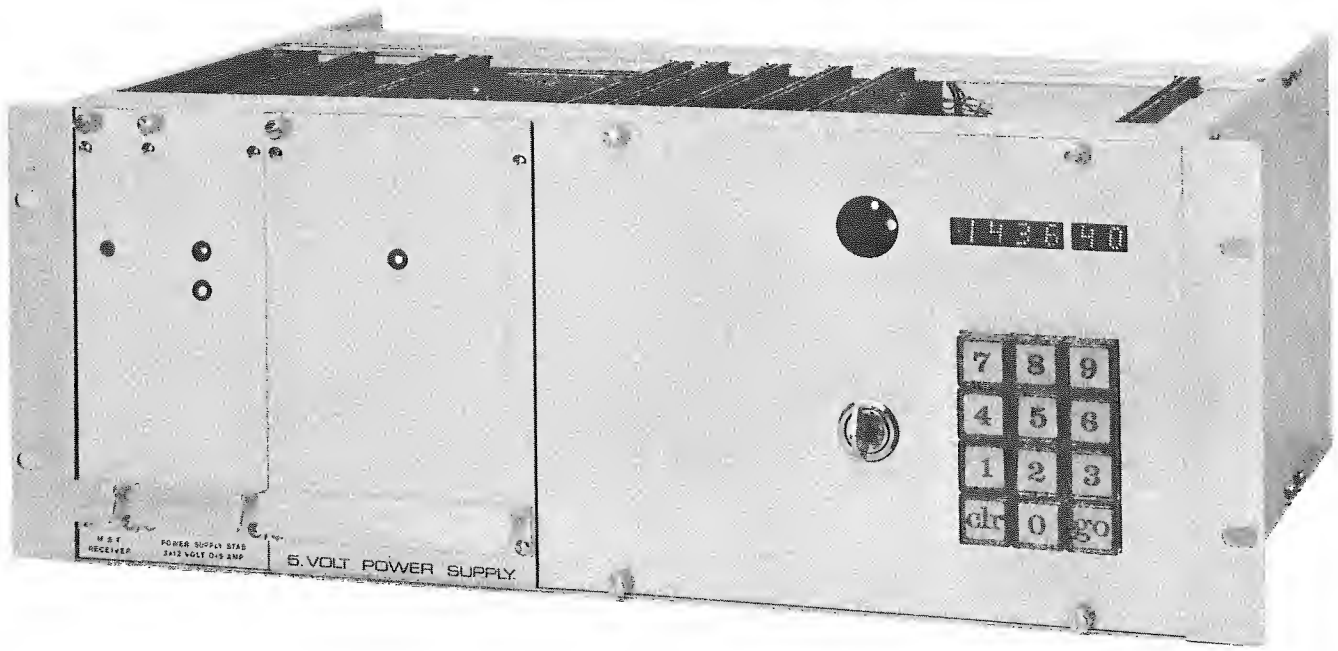

Fig. 2 - The prototype clock

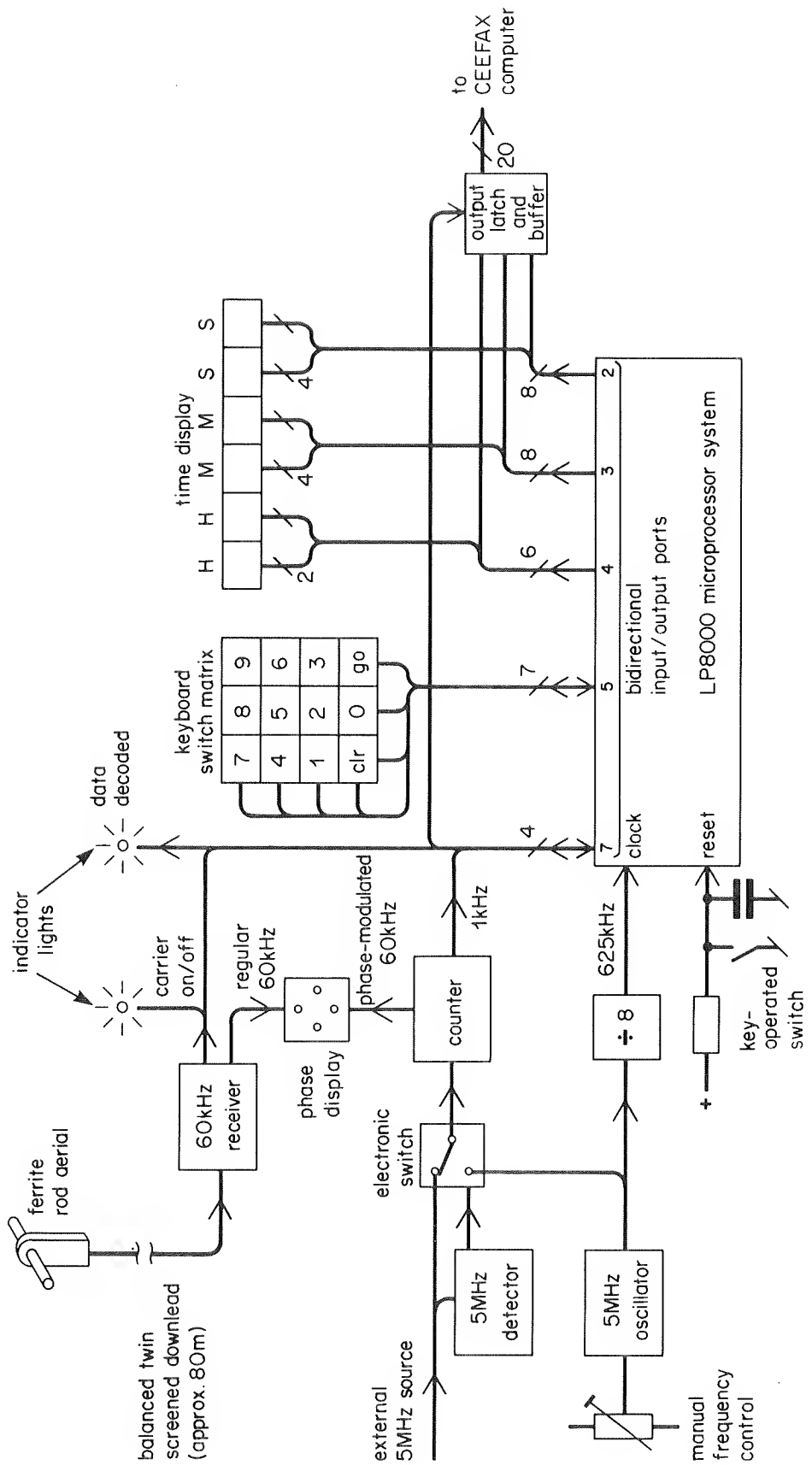

Fig. 3 - Block schematic diagram

absent, for example, during the regular MSF maintenance period (currently around noon on the first Tuesday of each month) the clock continues at the rate determined by the external 5 MHz source or, failing that, its internal oscillator.

Since the clock is required to generate British clock-time it responds to the particular bit indicating when BST is applicable although the response is necessarily late as that bit changes after the time itself should have changed.

An output is available indicating that a time code was decoded during the last minute. This can be used to discreetly alter the CEEFAX time display (by, for example, replacing the separator symbol ; by :) to signify to an observer that the time is reliable.

3. Block diagram

Fig. 3 illustrates the clock system which is based upon the LP8000 microprocessor. Groups of eight (or fewer) signal connections to the microprocessor constitute a port, the state of a port being described by an eight-bit byte handled within the microprocessor. The ports can serve as inputs and outputs. An output byte is always available at each port, but it is combined in a logic 'OR' operation with any external inputs. So to use a connection as an input, the corresponding output bit must be set at '0'; correspondingly, to use it as an output no input, or a '0' must be applied. The use of connections as both inputs and outputs is illustrated by the arrangement in which the seven lines of port 5 are connected to a 4 x 3 matrix of switches on a keyboard, as indicated in Fig. 3. The microprocessor can test which key is pressed, or whether more than one is pressed, by sending 1's on one set of lines and 0's on the other set while testing for 1's received as inputs on the latter set.

The operation of the microprocessor system is controlled by an internal clock of 6·4 μs period (the machine cycle) derived by counting the 625 kHz clock input. The microprocessor includes more than 50 bytes of read/write memory together with several hundred bytes of Read-Only-Memory (ROM) containing the program. During each machine cycle, one instruction byte of the programme ROM is made available, the byte being selected by an address stored in a read/write memory organised as a counter (the program counter). At the end of each machine cycle, the state of the read/write memory, including the output port registers, are functions of their states at the start of that cycle as modified by the effect of the instruction byte. The instruction bytes correspond to operations such as addition or shifting of bytes within the system. So the entire history of the system depends upon its inputs and its initial state, as controlled by the stored program of instruction bytes. In order to ensure a repeatable starting condition a reset input is provided, this is activated automatically on switching-on or it can be operated at any time by a key-operated switch.

It is beyond the scope of this report to list the instructions available in this microprocessor system, and the program developed for this particular application, but it should be clear that there is great flexibility in this approach. Within the limits of the inputs and outputs provided, and the number of machine cycles available to execute a function, many different functions can be performed. In particular, many modifications to the clock can be made solely by changing the 'software' in the program ROM without any alteration to the wiring of the unit. It is clearly useful to choose the inputs and outputs of a microprocessor system in such a way that foreseeable modifications or improvements can be made without the need to alter the 'hardware'.

The output bytes from ports 2, 3 and 4 are the hours, minutes and seconds in BCD. They change at different times as they are controlled by different instructions in the program. In order to present 20 parallel data streams, which change together, to the CEEFAX computer an output latch controlled by a strobe pulse from port 7 is used. The output data correspond to the next second and the timing of the strobe pulse (which occurs once every second) can be altered in the program to provide the desired advanced timing for the data. Typically the strobe is generated 300 ms before the seconds change to allow the CEEFAX time to be never late even after a delay of about up to a quarter of a second before the next page header carrying the time.

Apart from the keyboard (see Fig. 3) there are only two inputs to the microprocessor. One is the two-level signal from the 60 kHz receiver, which indicates whether the carrier is on or off, and the other is a 1 kHz reference frequency for the clock and time-code decoder, derived from the external or internal 5 MHz source.

The 60 kHz signal is received by a tuned ferrite-rod aerial mounted outside the building and coupled to the receiver using balanced twin cable and suitable matching. The receiver provides a two-level logic signal representing carrier on/off which is also coupled to an indicator light. The response time of the receiver/detector combination is about 2 ms. The receiver also provides a logic-level 60 kHz output for use in a phase comparator display.

The output from the internal 5 MHz crystal oscillator, with provision for manual frequency trimming, is counted down to give a 1 kHz reference frequency for the clock and data decoding. An intermediate stage of this counter gives an irregular 60 kHz signal. This signal is logically combined with the 60 kHz signal from the receiver to give a four-light phase display, one rotation representing one cycle. It is a simple matter to trim the oscillator to give a difference of less than one cycle is 15s, corresponding to a timekeeping error of less than 100 ms per day. The output from the internal 5 MHz oscillator is also divided by eight to give a stable 625 kHz clocking source to run the microprocessor.

When an external 5 MHz frequency reference is applied, it is tested to ensure that it has the required amplitude and frequency, with the particular need to reject 4·43 MHz colour subcarrier. When an acceptable external signal is present, it is selected automatically in preference to the internal 5 MHz which, however, con-

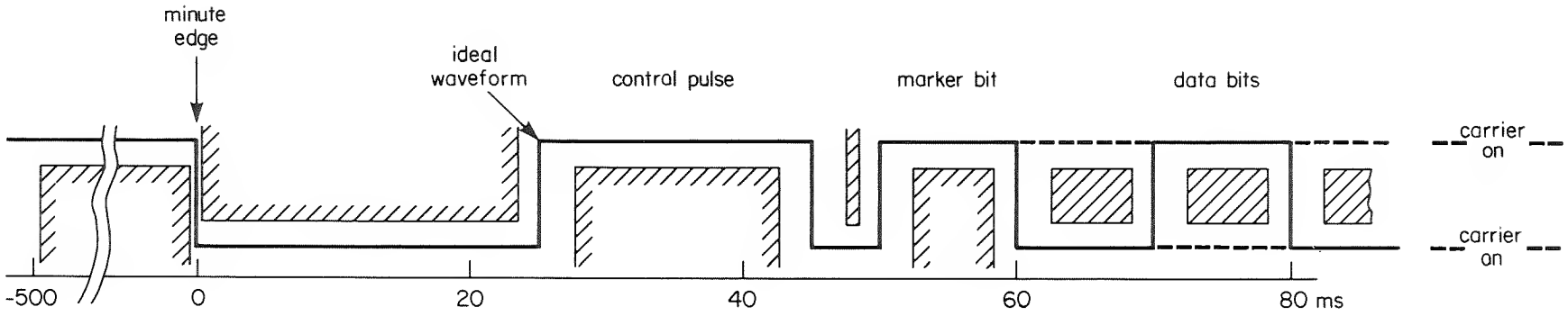

Fig. 4 - The waveform template

tinues uninterrupted to supply the 625 kHz to the microprocessor system. The electronic switching to and from the external source occurs within milliseconds and in such a way that any disturbance to the 1 kHz reference is such as to increase its period.

4. Principle of operation

There are four functions to be carried out by the microprocessor program, the clock itself, the output routines, the keyboard control and the time-code decoding. In every period of the 1 kHz input, each of these functions receives attention as necessary.

The count of the clock, which is stored in five bytes of the read/write memory, is incremented every millisecond. The counting is started by either a correctly decoded time-code or by pressing the 'go' key. Once the counting has started it can only be altered by correctly decoded time-codes or by resetting the entire apparatus by a lockable switch. The keyboard itself is inoperative during normal running of the clock. The clock within the microprocessor always operates on the UTC scale.

The hours, minutes and seconds of the clock, with the hours corrected when appropriate to BST, are available as BCD digits on parts 4, 3 and 2. At a fixed time during each second a 32 μs strobe pulse is produced and this is used to latch all these digits into the output register coupled to the CEEFAX computer. A further output indicates whether a time-code has been correctly decoded during the last minute.

The keyboard is interrogated every 10 ms until the clock has been started, after which the keyboard is ignored. The program requires a key to be depressed at two consecutive interrogations before action is taken; this is to eliminate contact bounce effects. The keyboard allows an initial time (hours, minutes, seconds) to be entered with provision for mistakes to be cleared and the clock to be started.

The time-code is examined by a very critical test intended to eliminate spurious responses to unexpected conditions. The two-level signal from the MSF receiver is examined every millisecond for the pattern indicated by the template in Fig. 4. Only a sequence completely satisfying this pattern of consecutive 1's 0's or 'don't care' conditions is accepted for interpretation as a time code. During the preamble the template defines the waveform uniquely, during the data bits the waveform must pass either above or below the data 'eye'. In addition to this, the parity checks of the data must be satisfied. A further provision in the program ensures that, except at the first correctly received time code after the start-up, two consecutive disagreements, a minute apart, between the time code and the clock are necessary before the clock is reset. This substantially eliminates the possibility of a false time-code reception due, for example, to the aerial being unplugged between data bits.

5. Software flexibility

It will be appreciated from the above description that many minor changes or improvements to the functions of the clock can be made by altering only the program stored in the Read-Only-Memory associated with the microprocessor.

For example, the mode of operation of the keyboard could be altered to allow step adjustments to be made to the clock time, or the timing of the seconds pulse, while the clock is running. Provision for the leap second could also be provided so that a 'flag' could be set and then cancelled at midnight UTC on 30th June or 31st December when the time 23.59.59 would be followed by 23.59.60 and only then by 00.00.00.

If a version of the clock were required to operate in a different time zone but using MSF transmissions or using an alternative two-level time code, the program could readily be adapted. At the time of writing the MSF transmissions include a 'slow' code (one bit per second) including additional information such as the day-of-week. This could be made available by software changes although additional outputs may also be required.

6. Conclusions

A microprocessor-based clock for use with the CEEFAX computer has been described. The unit has been in use for several months without any attention and it has kept the CEEFAX time correct within a fraction of a second except on isolated occasions when wrong time-codes have been transmitted from MSF. Considerable extra effort was required to develop the software for the microprocessor compared to the effort that would have been required to design and build a hardware system using perhaps fifty extra integrated circuits.

However, the microprocessor-based system provides the opportunity to modify the operation by software changes. There is insufficient evidence to judge the reliability of the microprocessor approach but as it uses fewer connections and less power it is likely to be at least as reliable as discrete logic counters and gates. Faults in the input or output devices could be rectified using conventional techniques but there would be considerable difficulty in identifying a fault within the microprocessor system itself.

Appendix

Time scales

The legal civil time in the British Isles is Greenwich Mean Time (GMT) or, when specified, British Summer Time (BST) which is exactly one hour in advance of GMT. Greenwich Mean Time is based on numerous observations of the sun's transit across the meridian collected, corrected and correlated over several years. It is a dynamic time scale, based on a variable unit. Although in GMT there are always 60 seconds in a minute, the length of the second varies gradually.

All the time references generally available, including the Greenwich Time Signal (GTS), the Post Office speaking clock, and the 60 kHz MSF Rugby time codes, are based on Co-ordinated Universal Time (UTC). This is based on the frequency of radiation corresponding to the transition between specified energy states of the Caesium 133 atom which is, by definition, taken to be 9 192 631 770 Hz. The seconds of UTC are always the same length, but there are not always 60 seconds in a minute. Under the control of the Bureau International de l'Heure (BIH) leap seconds are occasionally inserted, and, if ever necessary, deleted, in order to keep UTC within ±0·7s (usually) and ±0·9s (extreme tolerance) of UT1 (which, for the purposes of this note, can be taken to be equivalent to GMT). The difference between the two time scales, expressed in units of 100 ms, is broadcast as part of the MSF transmission pattern.

Although the software of the CEEFAX clock could readily be adapted to give true GMT (within about ±50 ms) it was thought more appropriate to give UTC, advanced by one hour during BST, to be consistent with the other time references available to the public.

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